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Docket No.: 116120US2

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 09/176,315
Applicants: Shigenobu MAEDA, et al.
Filing Date: October 22, 1998
For: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND RECORDING MEDIUM
Group Art Unit: 2811
Examiner: Crane, S.

SIR:

Attached hereto for filing are the following papers:

REPLY BRIEF UNDER 37 CFR §41.41, EVIDENCE APPENDIX
REQUEST FOR ORAL HEARING

Our credit card payment form in the amount of **$1,000.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Docket No. 116120US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Shigenobu MAEDA, et al.

SERIAL NO: 09/176,315 GAU: 2811

FILED: October 22, 1998 EXAMINER: Crane, S.

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REQUEST FOR ORAL HEARING

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant's representative hereby respectfully requests that an Oral Hearing be scheduled in the above-identified application.

A credit card payment in the amount of **$1,000.00** to cover the fee is enclosed herewith and any further charges may be made against the Attorney of Record's Deposit Account No. **15-0030**. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

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SHIGENOBU MAEDA ET AL.	: EXAMINER: CRANE, S.
SERIAL NO: 09/176,315	:
FILED: OCTOBER 22, 1998	: GROUP ART UNIT: 2811

FOR: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND RECORDING MEDIUM

REPLY BRIEF UNDER 37 CFR §41.41

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

The present Reply Brief is presented in order to point out and respond to numerous errors in the Examiner's Amendment (hereinafter EA) as to misstatements of fact and the failure of the PTO to either acknowledge or follow controlling precedent.

I. THE INVENTION AS A WHOLE

It is well established "that a patentable invention may lie in the discovery of the source of a problem" and that [t]his is *part* of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. 103." *See In re Sponnoble*, 405 F.2d 578, 585, 60 USPQ 237, 243 (CCPA 1969).

The PTO reviewing court recently reiterated the importance of consideration of the problem of concern in In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) as follows:

> In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. [Emphasis added.]

While the problem of concern in the prior art references being applied do not have to be the same problem, they must at least be similar problems that have the same solution, *See In re Wiseman*, 596 F.2d 1019, 1023, 201 USPQ 658, 661 (CCPA 1979). As explained in detail below, the problems of concern in the applied references are not similar problems to the **STABILITY** problem discovered by and of concern to Applicant's. Moreover, to the extent that solutions are offered to the problems discussed in these references, they are not the same solution that has been disclosed and claimed in terns of the design limitations set forth by base independent Claims 1 and 2.

The problem confronting the present inventors is clearly described in the specification at page3, line25 to page 4, line 5. This problem is **NOT** simply a matter of the speed of operation of the claimed SOI MOS transistor, instead; the concern is to provide **STABILITY** when operating SOI MOS transistors "in synchronism with a clock having an operating frequency of not less than 500 MZ . . . " (emphasis added). Further in this regard, it is clear that the only hint of this problem of **UNSTABLE** high speed operation when SOI MOS transistors of the nature indicated in the rejected claims are operated "in synchronism with a clock having an operating frequency of not less than 500 MZ" (emphasis added) appears in the disclosure in the instant specification (at page 4, lines 2-4, for example). Likewise, the only hint of a solution

to this problem is in the design criteria for the claimed SOI MOS transistor set forth by base independent Claims 1 and 2.

II. MISSTATEMENT OF THE CLAIMED INVENTION

As noted above, the problem is not simply "high speed" operation at a frequency of not less than 500 Mz as the PTO attempts to characterize it throughout[1] the EA. Instead, it is the **STABILITY** of operation "in synchronism with a clock having an operating frequency of not less than 500 MZ" (emphasis added), as noted above. However, instead of carefully considering the problem and the solution thereto that has only been disclosed in Applicants' specification, the PTO has endeavored to **MISSTATE** the very claim limitations that emphasize this subject matter in base independent Claims 1 and 2 in terms of the requirements therein for the claimed SOI MOS transistor to be "operated based on a predetermined clock," with transistor design including the steps of "providing an operating frequency of said predetermined clock" and "determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock" (emphasis added). Clearly, "clock" does not simply mean any drive frequency source and the specification does not use the term "clock" interchangeably with "operating frequency" as incorrectly alleged at page 4, lines 4-6 of the EA. Thus, the EA is in error in asserting that it is proper to rely upon a merely asserted interchangeable usage as a basis to then interpret the claim language requiring, for example, the claimed MOS transistor to be "operated based upon a predetermined clock" having an "operating frequency,"

[1] Note, for example, page 12, lines 1-5 that observes that the "structure of Iwamatsu et al. operates at its desired GHz frequency" while completely ignoring that the problem of concern is the stability of an SOI MOS transistor being operated "in synchronism with a clock having an operating frequency of not less than 500 MZ."

labeled as "f," as being simply any transistor driving source that can be said to supply a transistor operating frequency. .

In this last respect, and as noted above, the specification notes the problem of concern in this application as being the "high speed operation in synchronism with a clock having an operating frequency of not less than 500 MHz" (emphasis added) in the sentence bridging pages 3 and 4 thereof. As further noted at page 4, lines 1-5, this "high speed operation in synchronism with a clock having an operating frequency of not less than 500 MHz" (emphasis added) results in unstable operation of even fixed body potential SOI MOS transistors, like those taught by Iwamatsu and shown schematically in Fig. 23 of the present Application. While it is true that the specification sets forth no definition for the well understood term "clock," this is common practice as to such widely understood terms that does not give the PTO license to concoct a definition at odds with what those skilled in the art would consider to be a "clock." in terms of a device that can generate periodic signals having a highly precise fixed frequency[2]. Clearly, the specification does not teach or suggest anything but the standard meaning for a "clock" and does not suggest that a transistor is being driven by any source that can be said to provide an input frequency signal as the EA interprets "clock" at page 4, lines 9-11.

The situation here is not unlike that encountered by the court in In re Kotzab, 217 F.3d 1365 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) as to PTO allegations of equivalence of terms that were not actually equated by the reference disclosure that was there the concern. The court dismissed such allegations as lacking the required showing as to "substantial evidence" as the disclosure of the reference made no such

[2] See, for example, The IEEE Standard Dictionary of Electrical and Electronic Terms, 6th Edition, page 163.

equivalency statement just as the disclosure here does not equate the term "clock" to the `transistor operating frequency as urged in the above-noted portion of the EA.

Apparently aware that the term "clock" has been stretched beyond any reasonable elastic limit by the interpretation that it is simply any input device supplying the transistor an input frequency that could have some particular momentary value, page 4 of the EA then proposes (in lines 11-14) an alternative interpretation that again focuses on the abstract statement of Iwamatsu that "the maximum operation frequency is 2.1 vGHz at 3.3V" as if this were a statement that the "maximum operation frequency" is developed by a "clock," and does not just refer to an instantaneous frequency. While some source of an input signal must indeed be provided, it cannot simply be presumed that any input device would be a "clock."

The EA continues the same improper approach as to ignoring the standard meaning of the term "clock," and the problem noted in the application of attaining stable operation when a "clock" drive is used, by the further improper interpretation of the word "clock" in the two method steps treated at page 5, lines 7-15 thereof. Again, a "clock" is incorrectly read as any source of an input signal that can simply apply a signal to the transistor that has at least a frequency component that is at the claimed frequency of greater than or equal to 500MHz.

III. MISSTATEMENTS OF IWAMATSU TEACHINGS AND CLAIM LIMITATIONS

More importantly, even if one assumes, without the presentation of evidence, that a clock is a potentially good source to use as an input to the suggested frequency divider of Iwamatsu, and even assuming that the artisan would implement the suggested transistors of Iwamatsu using some kind of transistor "layout pattern," there

is clearly no teaching in Iwamatsu of any particular criteria for that "layout pattern." Moreover, while the NMOS transistors of Iwamatsui relied upon in the EA will have gates, body regions and body contacts, there is no suggestion in Iwamatsui of any of the factors that will determine a the gate capacitance for those MOS transistors or for the resistance of the fixed potential transmission path extending from any one body contact to any body region.

Furthermore the apparent concern in the paragraph bridging pages 5 and 6 of the EA diverge from proper PTO concerns as to patentability to incorrect appraisals as to determining if the claimed step of determining a layout pattern of the claimed MOS transistor ("based on the operating frequency of said predetermined clock, wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression $R \bullet C \bullet f<1$," with the claimed definitions of R, C, and f) would be infringed. Determining infringement is in the province of the federal judiciary, not the PTO. Moreover, the assertion of determining infringement is incorrect as the "R" is defined to be "the resistance of a fixed potential transmission path extending from said at least one body contact to said body region" which is something different than the transistor channel that serves as the "current path" referenced at line 22 on page 5 of the EA that is a path from the transistor drain to its source that is controlled by the gate as illustrated in Fig. 36 of the Sze text attached to the Appeal Breif (herein after AB) and reattached to this reply brief as an evidence appendix for the Board's convenience. Thus the EA appears to confuse the "current path" of a transistor and the "fixed potential transmission path" that is designed as essentially supplying equal potential, not current flow. Thus, the EA is in error as the RC time constant of the transistor "current path" is not what will determine infringement based upon the express words of Claims 1 and 2 that require the R of concern to be "the resistance of

a fixed potential transmission path extending from said at least one body contact to said body region" that has nothing to do with the "current path."

Also, as the subject matter of both independent base Claims 1 and 2 require a consideration of an "R= the resistance of a fixed potential transmission path extending from said at least one body contact to said body region," not the R of any current path, the statement at lines 3-4 on page 6 of the EA is incorrect in asserting that "because any current path that is designed to meet the limitation on the RC time constant would meet the claim limitation.

IV. NO REASONABLE MOTIVATION

The PTO reviewing court recently emphasized that a showing of a teaching or motivation to combine prior art references is a prerequisite to establishing a valid *prima facie* case of obviousness. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.)." This admonition was set forth by this court in even more precise terms in In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998) as follows:

> To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness.

However, the EA continues the above-noted incorrect assumption that the RC time constant for a "current path" is part of the claimed subject matter and adds misinterpretations as to the teachings of Chen to the design of a device with a

particular RC time constant for this "current path," instead of establishing the required showing of reasonable motivation.

In this last regard, the PTO appears to suggest that even though Iwamatsu is relied upon to teach operating at a particular frequency, part of the PTO suggested reason for modifying Iwamatsu that was urged to have the claimed operating frequency is that "one wants the device to actually operate at the frequencies it is designed for" as stated at lines 19-20 on the bottom of page 14 of the EA. This appears to be a contradiction that can hardly be offered as evidence or reasoning in support of establishing the required showing of motivation.

At page 6 of the EA, the PTO does little more than note that the teachings of Chen suggest that a device should be designed so that a "current path from the body region associated with a channel . . . to the body contact 39 is less than 1 nsec, apparently as to the disclosure of column 7, lines 25-34. Once again, the terminology "current path" is the creation of the PTO that does not fit anything reasonably taught by Chen. In this regard, those skilled in the art would have no reason to believe that the "body link" of Chen relates to the current path-channel 32 illustrated in Fig. 1 of Chen or anything illustrated to be above that channel such as the Fig. 1 illustrated gate 27 above the gate oxide 34 that is above each channel 32, see col. 3, lines 15-18 of Chen. Thus, the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) precludes any consideration of gate capacitance relative to the Fig. 1 illustrated gate 27 above the gate oxide 34 that is above each channel 32, at least to those familiar with the clear meaning of the words used by Chen.

The above-noted interpretation of this column 7, lines 25-34 actual teaching clearly inserts PTO interpretations that have no substantial evidence support in Chen. If the PTO is to continue to argue that Chen teaches the design of a device with a particular RC time constant for a "current path," it should point to the language in Chen being relied upon to teach a "current path" and not just a body contact in contact with a body to fix the body potential as the Rijckaert decision cited at page 16 of the AB[3] clearly requires.

Besides the clear lack of any teaching or suggestion in Chen that the suggested modification of he doping concentration in recessed region 20 to reduce the RC time constant in the body link or recessed region 20 to as short as 1 nsec, is a "design" step related to a "current path," there is also no teaching or suggestion to be found in Chen that equates the clearly illustrated and described[4] recessed region 20 of FIG. 1 to "the continuous sheet of Si which surrounds the N+ source and drain regions" that clearly includes all recessed regions 20 and all the mesas 24. Even though mesas 24 are not recessed in any way, the PTO continues to try to include them as somehow a part of the recessed regions 20. Again, the Rijkeart decision requires the PTO to show where and how Chen equates what are clearly individual recessed regions 20 illustrated in FIG. 1 and described as such throughout Chen to the "the continuous sheet of Si which surrounds the N+ source and drain regions" simply because of the top view showing of FIG. 3. I n this regard, the PTO reviewing court has made it clear that the PTO may not simply assert conclusions, it must explain how the reference supports the conclusion, the "full and reasoned explanation" required by In re Lee, 61 USPQ2d 1430, 1432-33 (Fed. Cir. 2002).

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[3] See In re Rijckaert, 9F. 3d 1531, 1533, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) ("When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference.").
[4] See column3, lines 5-18, for example.

Turning to Agari, the EA does no more than again note the wiring parts disclosed therein as signal conductors and try to find a relationship between the claimed "fixed potential transmission path extending from said at least one body contact to said body region" and these wires by again implying that a "body link" as in Chen is somehow to have the same RC considerations as a signal carrying conductive wiring, apparently again assumig the "body link" to be a "current path." However, any fixed potential "body link" of Chen is not such a "current path" and the attempted analogy clearly is without merit.

Not only does the EA fail to include a motivation rationale setting forth any sound technical reasons supporting the proposed reference modifications, the EA does little more than allege that the different references relied upon show some of the features set forth by the rejected claims to be "known," and based only upon this allegation of "known" status, the combination of these claimed features is asserted to have been in some way obvious. Note the discussion of Gunning, Masuda, and Agari at page 8, lines 5-18, the alternative theories of obviousness unsupported by any references at page 9, lines 10-12, and the discussion of Agari, Masuda, Gunning, Chen, and Iwamatsu in the summary at page 14 of the EA.

As has been previously noted, at page 15 of the AB, relative to In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998), for example, the case law requires the PTO to set forth the motivational reasons why the artisan would have been led to make reference modifications and not to just assert knowledge. This case also requires the PTO to present the reasons for even selecting the particular references, much less the disparate teachings from such clearly disparate references

In so far as the EA attempts to equate the showing of any particular feature to establish that feature as having been "known" as a substitute for the required

showings of the motivational reasons for selecting both the teachings from the reference s and the references themselves, Rouffet is further highly relevant. In this regard the Rouffet court observed (149 F.3d at 1357, 47 USPQ2d at 1457) that most if not all inventions arise from a combination of old elements, that every element of a claimed invention may often be found in the prior art and that such mere identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. However, such mere identification is at best what the PTO is asserting as at page 8, lines 10-18, and in the summary bridging pages 14-15 of the EA.

Once again, it appears that subjective conjecture is being substituted for evidence in terms of unreasonably lifting unrelated reference teachings from disparate references and then suggesting that these teachings would be combined simply because they represent what is "known." However, the question is what the references themselves reasonably suggest in terms of some reason to mix and match disparate teachings.

CONCLUSION

The bottom line here is that the PTO has failed to present any convincing reasoning, much less evidence, as to why the artisan would have some reason to consider the product of the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed and the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region to be important to incorporate in the layout design of a transistor. Similarly lacking is some prior art based reason to believe that this particular RC product having an R value determined by an interior body region and a C value

related to a gate electrode over an oxide layer of transistor should be minimized as to a clock signal period so as to produce some desired result. Consequently, the rejection as applied to Claims 1-5 and 18 should be reversed for the above-noted reasons and the reasons noted in the AB.

Respectfully submitted,

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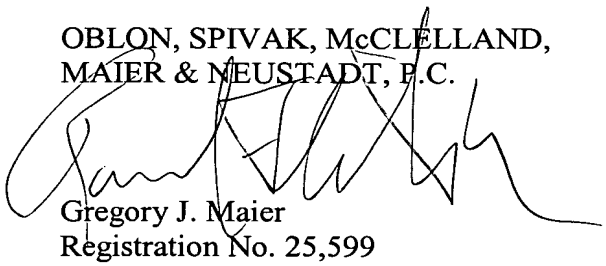

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EVIDENCE APPENDIX

SEMICONDUCTOR DEVICES

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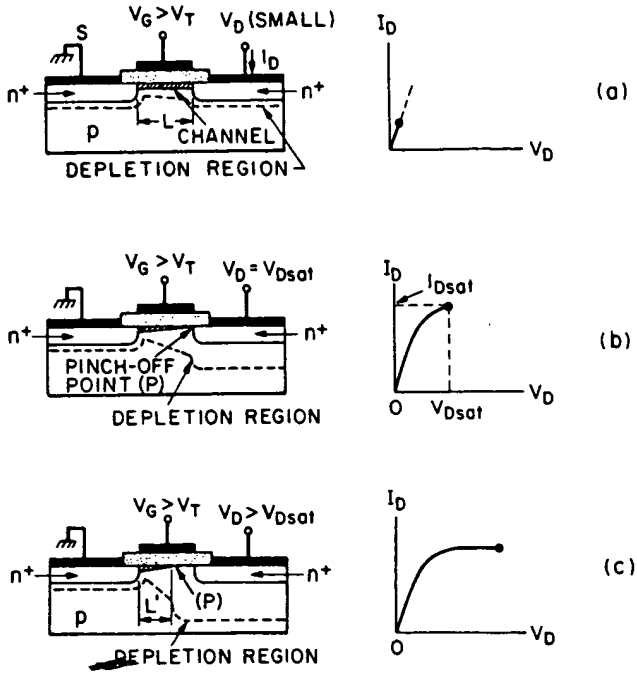

Fig. 35 Operations of the MOSFET and output I–V characteristics. (*a*) Low drain voltage. (*b*) Onset of saturation. Point P indicates the pinch-off point. (*c*) Beyond saturation.

tion is called the gradual-channel approximation and generally is valid for long-channel MOSFETs.

Figure 36*a* shows a MOSFET operated in the linear region. Under the above ideal conditions, the total charge induced in the semiconductor per unit area, Q_s, at a distance y from the source is shown in Fig. 36*b*, which is an enlarged central section of Fig. 36*a*. Q_s is given from Eqs. 65 and 66 by

$$Q_s(y) = -[V_G - \psi_s(y)]C_o \tag{77}$$

where $\psi_s(y)$ is the surface potential at y and $C_o = \epsilon_{ox}/d$ is the gate capacitance per unit area. The charge in the inversion layer is given by Eqs. 56 and 77:

$$\begin{aligned} Q_n(y) &= Q_s(y) - Q_{sc}(y) \\ &= -[V_G - \psi_s(y)]C_o - Q_{sc}(y). \end{aligned} \tag{78}$$

The surface potential $\psi_s(y)$ at inversion can be approximated by $2\psi_B + V(y)$, where $V(y)$ as shown in Fig. 36*c* is the reverse bias between the point y and the source electrode (which is assumed to be grounded). The charge within the surface depletion region $Q_{sc}(y)$ was given previously as

$$Q_{sc}(y) = -qN_A W_m \simeq -\sqrt{2\epsilon_s q N_A [V(y) + 2\psi_B]}. \tag{79}$$

Substituting Eq. 79 in 78 yields

$$Q_n(y) \simeq -[V_G - V(y) - 2\psi_B]C_o + \sqrt{2\epsilon_s q N_A [V(y) + 2\psi_B]}. \quad (80)$$

The conductivity of the channel at position y can be approximated by

$$\sigma(x) = qn(x)\mu_n(x). \quad (81)$$

For a constant mobility the channel conductance is then given by

$$g = \frac{Z}{L}\int_0^{x_i}\sigma(x)\,dx = \frac{Z\mu_n}{L}\int_0^{x_i} qn(x)\,dx. \quad (82)$$

The integral $\int_0^{x_i} qn(x)\,dx$ corresponds to the total charge per unit area in the inversion layer and is therefore equal to $|Q_n|$, or

$$g = \frac{Z\mu_n}{L}|Q_n|. \quad (83)$$

The channel resistance of an elemental section dy (Fig. 36*b*) is

$$dR = \frac{dy}{gL} = \frac{dy}{Z\mu_n|Q_n(y)|} \quad (84)$$

and the voltage drop across this elemental section is

$$dV = I_D\,dR = \frac{I_D\,dy}{Z\mu_n|Q_n(y)|} \quad (85)$$

where I_D is the drain current which is independent of y. Substituting Eq. 80 into Eq. 85 and integrating from the source ($y = 0$, $V = 0$) to the drain

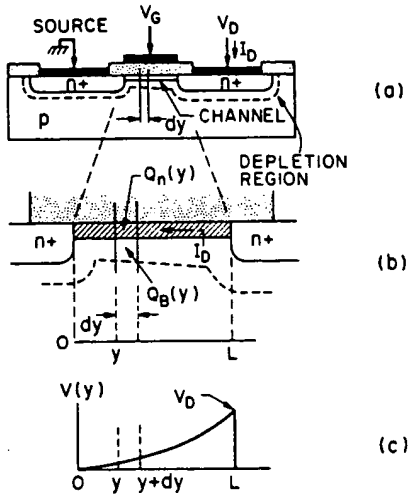

Fig. 36 (*a*) MOSFET operated in the linear region. (*b*) Enlarged view of the channel region. (*c*) Drain voltage drop along the channel.